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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/748,503	12/29/2003	Luke A. Johnson	42P18209	7288

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EXAMINER	
SHINGLETON, MICHAEL B	

ART UNIT	PAPER NUMBER
2817	

DATE MAILED: 02/10/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/748,503	JOHNSON ET AL.	
	Examiner	Art Unit	
	Michael B. Shingleton	2817	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 November 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-51* is/are pending in the application.

4a) Of the above claim(s) *51* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-50* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

MICHAEL B SHINGLETON
PRIMARY EXAMINER
GROUP ART UNIT 2817

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

Applicant's election of Species I in the reply filed on 11/16/2005 is acknowledged. Because applicant did not distinctly and specifically point out the supposed errors in the restriction requirement, the election has been treated as an election without traverse (MPEP § 818.03(a)).

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-5, 9, 14, 15, 20, 21, 23-27, 31, 36, 37, 42, 43 and 45-49 are rejected under 35 U.S.C. 102(e) as being clearly anticipated by Ishida et al. 6,711,084 (Ishida).

Figures 2, 3 and 5 and the relevant text of Ishida discloses a power on reset circuit/system (POR) and associated method having steps/structure of providing an ring oscillator 62 for "oscillating" and a counter 64 for providing a delay of the output of the oscillator or "oscillating" to provide a power on reset signal as is clearly illustrated in Figure 2 (Note the power on reset signal is also called a "POR" in Figure 2.). The delay unit being a counter and having flip-lops is clearly "logic that provides a delay in response to an input signal". Such a delay is the delay that is provided by counting. The counter, being that it is composed of flip flips that are recited as alternatives in the disclosed invention, is clearly a binary counter (See column 6, around line 43). Elements 74 and the like in the ring oscillator shown in Figure 3 are clearly inverters. In Figures 2 and 3 of Ishida note that the power on rest signal is provided to the NAND gate 72 so as to enable the ring oscillator. Figures 2 and 3 of Ishida also clearly show the NAND gate 72 as having an output connected to the input of the oscillator (Note the connection of the output of 72 to the input of 74.). The power on reset circuit or system is included in an electronic device namely a semiconductor device where one example is a DRAM (See column 3, around line 40 of Ishida). Also note Figure 1 of Ishida where the POR device/system/apparatus is part of the electronic device 1 and as

such the power on reset signal is provided within the electronic device. The DRAM circuitry includes a controller 44 (Note column 4, around line 62).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 6-8, 10-13, 22, 28-30, 32-35, 44, and 50 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ishida et al. 6,711,084 (Ishida) as evidenced by Gleichert et al. 5,347,547 (Gleichert).

Figures 2, 3 and 5 and the relevant text of Ishida discloses a power on reset circuit/system (POR) and associated method having steps/structure of providing an ring oscillator 62 for "oscillating" and a counter 64 for providing a delay of the output of the oscillator or "oscillating" to provide a power on reset signal as is clearly illustrated in Figure 2 (Note the power on reset signal is also called a "POR" in Figure 2.). The delay unit being a counter and having flip-lops is clearly "logic that provides a delay in response to an input signal". Such a delay is the delay that is provided by counting. The counter, being that it is composed of flip flips that are recited as alternatives in the disclosed invention, is clearly a binary counter (See column 6, around line 43). Elements 74 and the like in the ring oscillator shown in Figure 3 are clearly inverters. In Figures 2 and 3 of Ishida note that the power on rest signal is provided to the NAND gate 72 so as to enable the ring oscillator. Figures 2 and 3 of Ishida also clearly show the NAND gate 72 as having an output connected to the input of the oscillator (Note the connection of the output of 72 to the input of 74.). The power on reset circuit or system is included in an electronic device namely a semiconductor device where one example is a DRAM (See column 3, around line 40 of Ishida). Also note Figure 1 of Ishida where the POR device/system/apparatus is part of the electronic device 1 and as such the power on reset signal is provided within the electronic device. The DRAM circuitry includes a controller 44 (Note column 4, around line 62).

The counter of Ishida shown in Figure 5 includes T flip-flops. Ishida is silent on calling these flip-flops "latches". Column 4 around line 30 of Gleichert discloses that a T flip-flop is commonly referred to as a ""T" latch, flip-flop 125". Thus the T flip-flops of Ishida are seen as a latch. Note that page 4, in paragraph [0014] of the instant specification, the flip-flop is either recited as an alternative to

the latch or that the latch is also known as a flip-flop. However, the use of latches to make up a counter is conventionally known in the art as a well-known art recognized equivalent structure. The EXTPOR signal causes the most significant bit of the flip-flops of the counter to favor a known state. It would have been obvious to one having ordinary skill in the art at the time the invention was made to replace the flip-flops of Ishida with latches since the examiner takes Official Notice of the equivalence of a latch and a flip-flop for their use in the electronic art and the selection of any of these known equivalents to provide the counting or delay function would be within the level of ordinary skill in the art.

With respect to claims like claim 22 here the "apparatus is includes in an electronic device and the power-on reset signal is provided externally from the electronic device". The arrangement of Ishida also includes a power on reset apparatus 60 that provides the external power-on reset signal recited by the claims. Ishida, however, is silent on the details of the construction of the power on reset device 60.

Ishida does disclose one conventionally known form of power on reset device 56 as clearly illustrated in Figures 2, 3 and 5.

Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have replaced the convention power on reset device 60 of Ishida with on that is clearly illustrated in element 56 of Ishida because as the Ishida reference is silent on the exact exact structure of the power on reset device of element 60 one of ordinary skill in the art would have been motivated to use any art-recognized equivalent power reset device for element 60 such as the poser on reset device as illustrated by element 56 of Ishida.

In the invention made obvious above the consequence of the invention made obvious above is that the EXTPOR signal will cause the most signification bit of the latches of the counter to favor a known state. Now also in the invention made obvious above with the power on reset circuit 60 being composed of the same circuitry as that of power on reset circuitry 56 the consequence of the combination made obvious above is that the elements of the delay unit and the oscillator are chosen to have similar power-on behaviors. The "library" is a broad term that has no specific definition in the original specification of the disclosed invention. However, the elements that make up the device made obvious above come from known elements, i.e. transistors, flip-flips, etc. which are all stored in some "library" somewhere. Known elements are known primarily because they are recorded in a "library". The elements in a library were clearly utilized to design the electronic circuit of Ishida.

Claims 16-19 and 38-41 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ishida et al. 6,711,084 (Ishida) in view of Horn "Basic Electronics Theory" page 378.

Figures 2, 3 and 5 and the relevant text of Ishida discloses a power on reset circuit/system (POR) and associated method having steps/structure of providing an ring oscillator 62 for "oscillating" and a counter 64 for providing a delay of the output of the oscillator or "oscillating" to provide a power on reset signal as is clearly illustrated in Figure 2 (Note the power on reset signal is also called a "POR" in Figure 2.). The delay unit being a counter and having flip-lops is clearly "logic that provides a delay in response to an input signal". Such a delay is the delay that is provided by counting. The counter, being that it is composed of flip flips that are recited as alternatives in the disclosed invention, is clearly a binary counter (See column 6, around line 43). Elements 74 and the like in the ring oscillator shown in Figure 3 are clearly inverters. In Figures 2 and 3 of Ishida note that the power on rest signal is provided to the NAND gate 72 so as to enable the ring oscillator. Figures 2 and 3 of Ishida also clearly show the NAND gate 72 as having an output connected to the input of the oscillator (Note the connection of the output of 72 to the input of 74.). The power on reset circuit or system is included in an electronic device namely a semiconductor device where one example is a DRAM (See column 3, around line 40 of Ishida). Also note Figure 1 of Ishida where the POR device/system/apparatus is part of the electronic device 1 and as such the power on reset signal is provided within the electronic device. The DRAM circuitry includes a controller 44 (Note column 4, around line 62).

Ishida fails to show a buffer "included in the delay unit" and coupled at an output of the delay unit to provide the power-on reset signal.

The use of buffers in a circuit so as to provide isolation, increase the number of devices the circuit arrangement can drive, etc. is conventionally known See Page 378 of Horn.

Thus it would have been obvious to one of ordinary skill in the art at the time the invention was made to have provide a buffer at the output of the delay unit and thereby include the buffer in the delay unit so as to allow for the device to drive may more devices that would not be possible should the buffer not be present as taught by Horn (See page 378 of Horn).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael B. Shingleton whose telephone number is (571)272-1770.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Pascal, can be reached on (571)272-1769. The fax number for the organization where this application or proceeding is assigned is (571)273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

MBS
January 26, 2006

Michael B Shingleton
Primary Examiner
Group Art Unit 2817